SHARED RESEARCH AND DEVELOPMENT PROGRAM

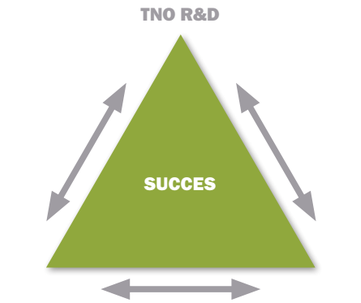
We invite you to join TNO in shaping the future of high throughput SPM.
We pursue an shared development model where technology is developed in technology programs and where the use of technology is demonstrated in integration programs.
Minimizing the step from research to innovation.
And where partners have maximum benefit from their R&D efforts and investments.

POTENTIAL APPLICATIONS

The number of potential applications of high throughput SPM is numerous.
We envision realizing concrete results for your business, e.g.

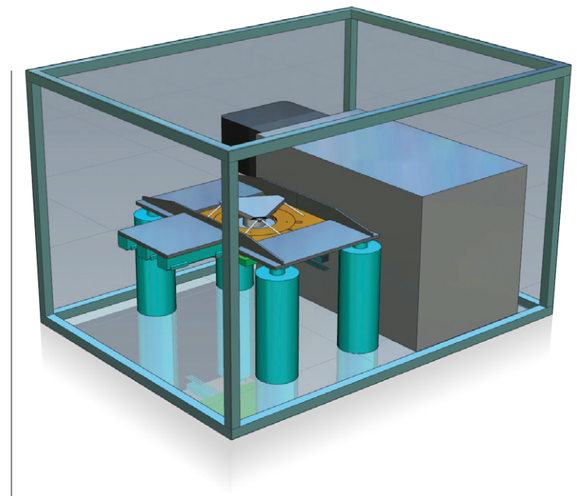
> Proof of Principle
> Functional Model
> Demonstrators
> Small-scale production
> Prototype equipment
> Your new products for technical evaluation
> Your new products for market probing

INNOVATIONS TO MARKET: THE VALUE CHAIN APPROACH



TOWARDS HIGH THROUGHPUT SPM

FOR SUB-10 NM DEFECT INSPECTION & PROCESS CONTROL



TNO innovation for life

TNO.NL

CONTACT
De Rondom 1
5612 AP Eindhoven
The Netherlands

T +31 (0)888 66 42 86
E patrique.boerboom@tno.nl

YouTube
Check our innovation videos:
www.youtube.com/user/TNOResearch

PROPOSAL FOR SHARED RESEARCH AND DEVELOPMENT PROGRAM HIGH THROUGHPUT SCANNING PROBE MICROSCOPY (SPM) FOR SUB-10 NM DEFECT INSPECTION & PROCESS CONTROL

2013/02/sft

TEAM UP WITH TNO TO MAKE THE FUTURE OF HIGH THROUGHPUT SPM FOR INSPECTION AND PROCESS CONTROL HAPPEN

INTRODUCTION

Due to the ever increasing metrology requirements for 1X nm node fabrication, measurements of sub-10 nm defects are required and recognized as one of the challenges for blank and patterned wafers and masks.

These metrology requirements are not yet being appropriately met by existing techniques, since they are already performing at the edge of their performance.

Scanning probe microscopy (SPM) has been suggested as one of the technologies that can fulfil the future metrology and inspection requirements, because it has the distinct advantage of being able to discern in 3D the atomic structure of the substrate.

TNO has an excellent technology which enables operation of many miniaturized SPM heads on a relatively large sample, such as a wafer or mask which enables a ground breaking increase in SPM throughput.

WHY?

- **Comply to ITRS metrology roadmap**
- **Enabling High Throughput SPM (>7 wafers/hour @450 mm*)**
- **Fulfil the requirements for future industrial metrology and inspection**
- **Prevention of contamination during metrology**
- **Easy & fast measurement of complex nanostructures**

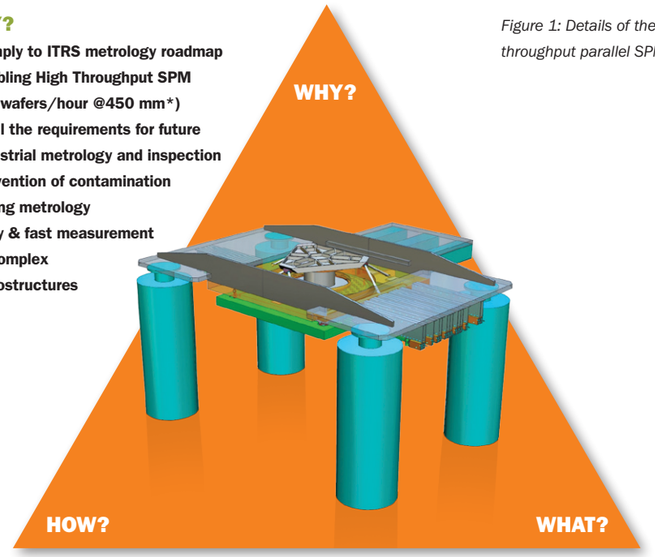


Figure 1: Details of the high throughput parallel SPM.

HOW?

- **50 parallel, miniaturized, SPM scan heads**
- **A revolutionary mechatronics positioning system for positioning and fixing mini SPMs**
- **Automatic probe exchange unit**
- **High performance wafer stage with wafer clamp**
- **Wafer handler for aligning, loading and unloading**
- **Calibration facilities and environmental conditioning**

WHAT?

- **Defect Inspection on Semicon Bare wafers and Blank masks (sub-10 nm up to 2 µm)**
- **Defect Inspection on Semicon patterned wafers (sub-10 nm up to 2 µm)**
- **Defect Review on Semicon Bare wafers and Blank masks (@1 nm lateral resolution)**
- **Defect Review on Semicon patterned wafers (@1 nm lateral resolution)**
- **Process controls such as CMP, Etch depth, roughness**

The trend

In electronics:

- Need for defect free IC
- Decreasing feature size (22 nm towards 10 nm Node)
- Wafers are getting bigger
- Equipment should be better designed to avoid contamination
- Increase in complexity and performance level of devices

In metrology:

- Throughput of current state-of-the-art SPMs are extremely low
- Increased metrology requirements @nano scale
- Amount of necessary metrology steps is increasing, it needs to be fast and simple

The offer

- **Nano scale metrology solution**
- **High Throughput SPM (>7 wafers/hour @450 mm*)**
- **Excellent contamination control metrology**
- **Easy & fast measurement of complex devices**
- **Invitation to become a member of the shared research and development program**

**Indication for Semicon Bare wafers/Blank masks, Scan site: 10 × 10 µm² (extendable to 100 × 100 µm²) , Scan sites/wafer: 50, resolution: 1 nm x 1 nm x 1 nm.*

TOWARDS HIGH THROUGHPUT SPM FOR INSPECTION AND PROCESS CONTROL

OUR VISION

The concept has been designed based on the requirements for defects inspection and review applications, but it can also be implemented for other process control and metrology applications.

It consists of two critical sub-systems; a parallel positioning mechatronics system (Figure 2) and miniaturized SPM heads. The current state of the art SPM heads were modified to become sufficiently small, simpler in terms of the architecture and increasing the bandwidth of their feedback system.
The positioning system (Figure 3) is capable of fast and accurate positioning of the SPM heads in targeted locations, and keeping the scan head stationary during the scanning operation.

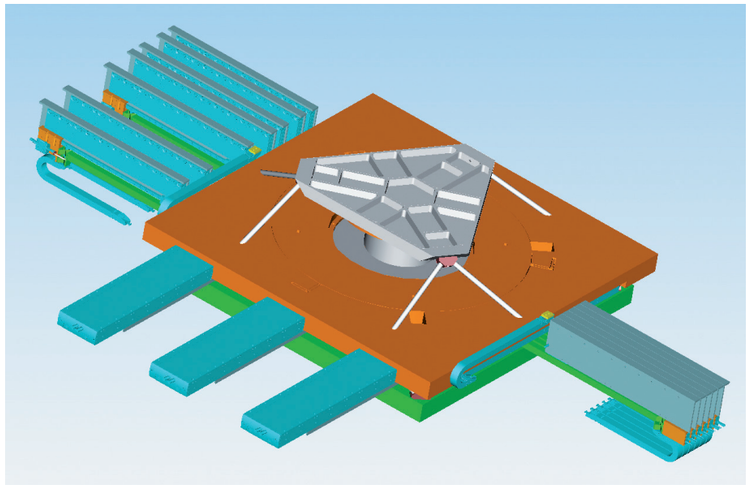


Figure 2.

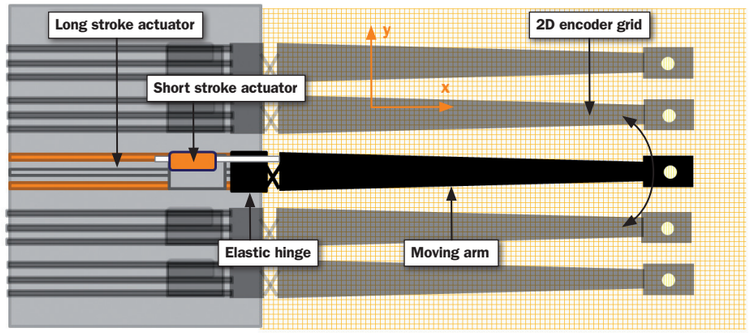


Figure 3.

Based on the roadmap for defect review tool requirements are shown in (Figure 4). TNO aims for an introduction in the high volume market in 2017 and a node of < 14 nm as for this no solutions are currently available.

SPM technology is already in use in semiconductor manufacturing but not for in-line inspection due to the throughput constraints.

KEY SPECIFICATIONS

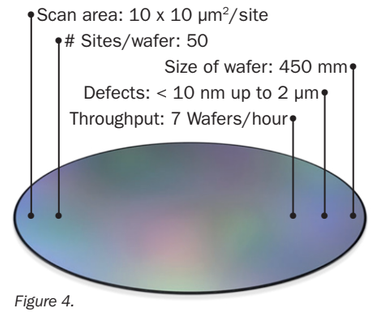


Figure 4.

OUR AMBITION: TO JOINTLY DEVELOP WORLD'S FASTEST SCANNING PROBE MICROSCOPE OPERATING AT HIGH RESOLUTION FOR LARGE SAMPLES