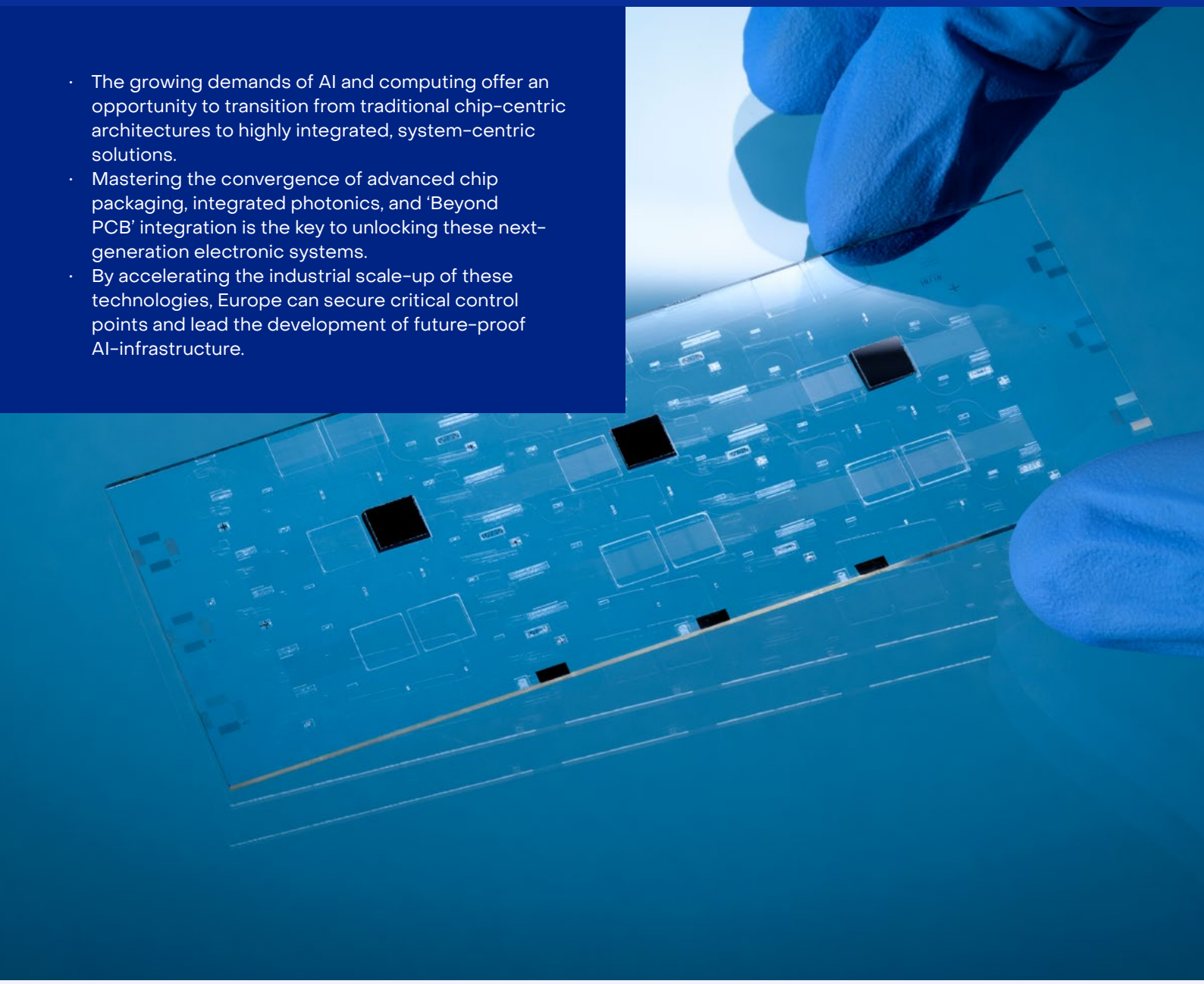
Future electronics

Beyond PCB and Chips

The invisible revolution in electronics and the opportunities for Europe

- The growing demands of AI and computing offer an opportunity to transition from traditional chip-centric architectures to highly integrated, system-centric solutions.
- Mastering the convergence of advanced chip packaging, integrated photonics, and 'Beyond PCB' integration is the key to unlocking these next-generation electronic systems.
- By accelerating the industrial scale-up of these technologies, Europe can secure critical control points and lead the development of future-proof AI-infrastructure.



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With strategic control in electronics shifting, Europe and the Netherlands must move from a chip-centric industrial policy to a system-centric strategy. This is not a policy preference but a technical necessity: AI workloads are pushing electrical interconnects to their limits, driving system complexity away from circuit boards and into tightly integrated architectures. This paper focuses on three converging responses: advanced chip packaging, integrated photonics, and 'Beyond PCB' technologies and the industrial roadmap needed to secure Europe's future position. It proceeds in three steps: identifying the architectural pressures from AI, energy, and scaling; showing how these pressures concentrate in new integration layers; and explaining why these layers constitute Europe's next strategic control points.

By 2035, electronics will no longer advance primarily by adding more connected devices, but by becoming an invisible, intelligent layer embedded throughout the physical world. The rapid rise of AI is accelerating this shift: sensing, computing, and decision-making are increasingly distributed across machines, infrastructure, and environments, operating continuously and often autonomously. This emerging AI-driven electronics layer is not primarily visible to users, but it is essential to how society functions, enabling real-time interaction between the digital and physical worlds at unprecedented scale.

Historically, major infrastructure revolutions followed a similar pattern. Electricity became transformative only once it disappeared into walls and machines, no longer experienced as a novelty but as a basic condition of modern life. Digital connectivity followed the same path, receding into the background as an alwaysavailable service. Toward 2035, electronics undergoes a similar transformation. It does not become less important; it becomes more essential precisely because it becomes embedded everywhere.

As electronics becomes an invisible but indispensable societal infrastructure, dependence on its reliability, performance, and evolution deepens across virtually all sectors. In this context, technological change no longer merely reshapes product markets; it redistributes economic power, strategic autonomy, and long-term competitiveness. As in earlier infrastructure revolutions, architectural shifts create new control points, hard to replace positions in global value chains producing winners and losers at the system level. This logic underpins Europe's post-Draghi competitiveness agenda: rather than pursuing full self-sufficiency, semiconductor policy prioritizes technological sovereignty, security of supply, and sustainability by seeking indispensability in those value-chain segments where Europe can credibly lead.

1. The Structural Break: Relocating System Complexity

The defining architectural change toward 2035 is not miniaturization alone, but a decisive relocation of where functional integration occurs. For decades, electronic system roadmaps were dominated by transistor scaling, while packaging and board-level integration were treated as supporting disciplines. As Moore's Law continues with diminishing returns, performance and energy efficiency increasingly depend on how chips are integrated, elevating packaging and interconnects from downstream steps to central architectural concerns.

AI as the Driver

Both AI training and inference drive integration pressure, but in different ways. Training stresses high-bandwidth, energy-efficient scaling across large clusters, while inference increasingly pushes dense, low-latency integration close to sensors, memory, and edge compute. In both cases, the dominant constraint shifts from compute capability to data movement, power delivery, and thermal management; domains where packaging, photonics, and heterogeneous integration become decisive. Similar constraints have long been visible in telecom and wireless datacenters, but AI scales these challenges across far broader system classes.

As copper interconnects approach their limits in bandwidth density and energy efficiency, particularly across board-level distances and connectors, traditional PCB-centric system architectures become increasingly inefficient. The issue is not engineering quality but architectural mismatch: printed circuit boards were never designed for the interconnect density, power delivery, and thermal coupling demanded by AI-scale systems. While copper remains effective over short distances, its energy cost per bit rises sharply at higher data rates, and signal integrity degrades as distances and connector counts grow.

Each additional PCB layer or connector adds loss, cost, and failure risk; penalties that become prohibitive at scale. Attempts to compensate by integrating ever more functionality onto a single monolithic chip have likewise reached practical limits: large dies no longer scale favorably in energy efficiency, yield, cost, thermal management, or design complexity. Together, these constraints are driving a shift away from both PCB-centric architectures and monolithic integration toward new system-level integration approaches.

System-in-Package (SiP) and Heterogeneous Integration

As traditional PCB-level integration approaches its limits, neither simply placing more chips on a board nor continued scaling toward ever-larger monolithic dies remains a viable path for performance- and energy-critical systems. The industry response is therefore a structural shift away from relying primarily on board-level and single-die integration toward much deeper integration at the package level. System-in-Package architectures, long established within More-than-Moore domains, are now expanding from specialized applications into a central system-level integration paradigm for high-performance and AI-driven systems. Multiple chiplets, memory stacks, sensors, RF components, and increasingly photonic elements are integrated into tightly coupled assemblies that function as complete systems.

Heterogeneous integration enables this transition. Instead of forcing all functions into a single manufacturing technology, heterogeneous integration allows each function to be manufactured in the most suitable technology, and then physically combined through advanced stacking or side-by-side integration within the package. Architectural differentiation therefore shifts away from transistor scaling alone toward interfaces, interconnect density, and package-level system design.

The result is a structural redistribution of complexity: away from monolithic chips and traditional boards, and toward package-level integration, chip-to-chip interfaces, and heterogeneous stacking. The package increasingly becomes the system's physical and architectural core. Although this shift may resemble earlier transitions from discrete components to integrated circuits, it is fundamentally different. Then, complexity was largely absorbed within a single chip. Today, it is spread across multiple specialized chips and re-integrated at the package and surrounding integration layers, where electrical, optical, thermal, and mechanical constraints must be co-designed. This relocation of complexity is decisive. It shapes not only system performance and energy efficiency, but also where economic value, margins, and strategic leverage emerge across the value chain.

2. Three Converging Technological Pillars

The future electronics landscape is defined by the convergence of three mutually reinforcing technological trajectories. These are not isolated developments, but interdependent elements of a single architectural transition.

1. Integrated Photonics (Light as the Core)

Initially adopted for long-range telecom and data communication, AI workloads now make photonics a necessity rather than an option even for short range interconnects. This is just one example of how Integrated photonics is increasingly adopted for shorter range data transfer over copper interconnects.

As data rates rise and energy budgets tighten, optical links are pulled ever closer to compute: from board-level optics to co-packaged optics and ultimately chip-level optoelectronic integration. Optical interconnects transmit far more data at significantly lower energy per bit than electrical links, especially at system scale, where hundreds to thousands of high-bandwidth links must operate within tightly constrained power and thermal budgets.

Integrated Photonics also plays a growing role in sensing and data communication modalities such as lidar, biosensing and optical wireless communication. These applications have existed for decades, but their tight integration with electronics, compute, and packaging has fundamentally changed system architectures, enabling smaller, cheaper, and more scalable solutions across mobility, robotics, healthcare and laser satellite communication.

The focus has shifted from making individual photonic devices work to the complex task of integrating and manufacturing them at scale. This is because photonics uses a mix of different materials, each chosen for what it does best. It combines silicon (common in computer chips), silicon nitride for guiding light, and special light-emitting materials like indium phosphide, all working closely together with electronic circuits on the same or connected chips.

2. Advanced chip packaging (The New System)

Advanced chip packaging is now the primary enabler of heterogeneous integration. Chiplets, co-packaged optics, functional integration, and 3D integration shift value creation from both the board and the individual IC toward the package level. In this paradigm, the package is the system, electrically, optically, thermally, and mechanically. Performance, energy efficiency, reliability, and manufacturability increasingly depend on integration quality at this level.

Advanced chip packaging does not uniquely introduce integration risk, but it redistributes and amplifies co-dependence across design, fabrication, assembly, and testing. While interface standardization mitigates some risks, yield learning, test strategies, and responsibility allocation increasingly hinge on package-level execution.

Packaging thus becomes a strategic industrial capability rather than a downstream step, requiring robust yield at scale, new test and metrology for heterogeneous systems, and viable value-chain models that allocate risk across design, fabrication, packaging, and testing. This transformation also deepens interdependence across the semiconductor ecosystem. An advanced chip package cannot be manufactured if even one critical component or technology is unavailable. As a result, chip designs become more specialized, supply chains more synchronized, and coordination across foundries, OSATs, equipment suppliers, and designers becomes a structural requirement rather than an operational choice.

3. Beyond PCB: Two Structural Integration Paths

As system complexity migrates away from traditional board-level assembly, “Beyond-PCB” integration does not describe a single technological direction. Instead, it captures two distinct but complementary structural shifts, each driven by different constraints and application needs.

Path A: From Board-Level Integration to Package-Level Integration (Performance-driven)

In high-performance and AI-driven systems, the primary limitation is no longer computation itself, but data movement, power delivery, and thermal management. To address these constraints, fine-pitch interconnects and high-bandwidth links are increasingly pulled upward from the PCB into advanced chip packages.

Technologies such as 2.5D interposers, 3D stacking, chiplets, and co-packaged optics relocate electrical and optical interconnects into compact multichip assemblies optimized for performance and energy efficiency. In this paradigm, the PCB does not disappear, but its role is reduced: it primarily provides mechanical support, coarse-pitch connections, and power distribution, while the critical system integration work occurs at the package level.

This transition marks a structural shift in how electronic systems are engineered. System performance, efficiency, and reliability increasingly depend on package-level design, interfaces, and assembly quality rather than on board-level wiring alone.

Path B: From Rigid PCBs to Thin, Flexible, and Printed Electronics (Product-driven)

A second, independent Beyond-PCB trajectory emerges in applications where product integration, comfort, weight, form factor, and sustainability dominate system requirements. Here, traditional rigid PCBs are replaced by thin, flexible, or printed electronic substrates that can be directly integrated into products and materials.

Additive and printed electronics, often manufactured using roll-to-roll processes, enable electronics to conform to curved or flexible surfaces and to be embedded into textiles, plastics, or structural components. This approach reduces material use, simplifies assembly, and opens new product categories, for example comfortable wearable health patches, smart packaging, and large-area sensing surfaces.

Unlike performance-driven package-level integration, this trajectory prioritizes manufacturability at scale, mechanical integration, and sustainability. It represents a fundamentally different architectural logic, even though both paths reduce reliance on traditional PCB assemblies.

Early Application Anchors

Both Beyond-PCB trajectories already show early industrial anchoring. In performance-driven systems, demand originates from AI compute infrastructure, high-speed communication, and heterogeneous computing platforms. In product-driven integration, anchors emerge in domains such as remote patient monitoring, wearable healthcare, logistics, and large-scale sensing, where thin, conformable electronics enable functionality that rigid PCBs cannot deliver.

Together, these twin shifts redefine the role of the PCB, not by eliminating it, but by differentiating where and why integration occurs within future electronic systems.

3. Sustainability as an Architectural Constraint

The scale implied by ubiquitous electronics, often described as a “trillion-sensor economy”, fundamentally challenges traditional system architectures. Replicating today’s electronics paradigms at that scale would imply a comparable proliferation of PCBs, connectors, housings, and discrete assemblies, driving disproportionate growth in material use, chemical processing, energy consumption, and e-waste.

Sustainability therefore cannot be addressed as a downstream optimization of existing designs. It becomes a first-order architectural constraint. The dominant sustainability gains arise from where functionality is placed in the system hierarchy, not merely from cleaner processes or marginal efficiency improvements. Concentrating complexity into highly integrated chips and packages reduces the number of interconnects, materials, and assembly steps required at system level.

This architectural shift enables sustainability on multiple fronts. Optical interconnects reduce energy consumption per transmitted bit as data volumes scale. Advanced chip packaging consolidates functionality into fewer, reusable units, lowering overall system material footprint and enabling longer product lifetimes. In parallel, Beyond-PCB approaches, such as embedded and printed electronics, allow functionality to be integrated directly into structural substrates using additive processes, reducing material waste and simplifying recycling through more homogeneous material stacks. Future flexible and printed electronics may also improve circularity through lower material use and new recyclable substrate concepts, although end-of-life processing remains an active area of innovation. The sustainability challenge in electronics is therefore structural rather than incremental. It depends primarily on system architecture, where functionality is placed and how integration is organized, rather than on incremental efficiency gains or cleaner versions of existing processes. By concentrating complexity where it can be controlled and designed for energy efficiency and circularity, electronics can scale without proportional growth in material use. Ubiquitous electronics will be sustainable only if system architectures are redesigned accordingly.

4. Strategic Imperatives for Europe and the Netherlands

As emphasized in the Draghi report and the EU's semiconductor strategy, Europe's long-term competitiveness increasingly depends on holding indispensable positions, Control Points, in selected parts of the value chain across design, manufacturing, and packaging. While advanced chip design and fabrication remain essential, industrial relevance is increasingly shaped by how chips are combined into complete systems. Leadership therefore no longer comes only from excellence in individual components, but from the capability to integrate them effectively into higher-level system solutions. Leaders in advanced logic, AI accelerators, and specialized architectures such as inference-optimized or neuromorphic designs, will remain dominant. However, their system-level impact increasingly depends on access to advanced chip packaging, photonic interconnects, and testing capabilities. Long-term strategic power no longer rests primarily with those who manufacture individual components, but increasingly with actors that occupy indispensable positions in the integration layers that bind complete systems together. This raises a critical strategic tension between vertically integrated players and disaggregated ecosystems, and between foundries extending into advanced chip packaging and OSATs moving upstream.

New Control Points

As packaging and integration become the primary drivers of system performance and efficiency, chips themselves are commoditizing into building blocks, with competitive differentiation moving to how these chips are connected, packaged, and deployed at scale. Long-term strategic relevance moves away from individual chips and toward control over the package-level integration capabilities that determine performance, energy efficiency, reliability, and manufacturability across entire value chains. Future control points will not primarily reside within individual technologies such as photonics, packaging, or Beyond-PCB. Instead, they increasingly arise in the capability to integrate these technologies into manufacturable, high-performance systems. For Europe and the Netherlands opportunities arise in four domains:

- System-level integration platforms, including architectures, co-design frameworks, and integration rules that enable heterogeneous systems
- High-performance optical and electrical interconnect technologies, including photonic coupling
- Test, metrology, and qualification capabilities for heterogeneous systems
- Enabling equipment and manufacturing systems for hybrid integration, photonic assembly, and in-line metrology

Existing Strengths

Europe, and the Netherlands in particular, holds strong positions in integrated photonics, advanced chip packaging, and enabling front- and back-end equipment. While most high volume semiconductor advanced chip packaging facilities are currently concentrated in East Asia, particularly Taiwan, photonics and next-generation package integration remain inherently multi-material and process-intensive. This aligns well with Europe's strengths in hybrid integration, equipment, and specialized manufacturing. Strategic relevance will therefore not be achieved through chips alone, nor by replicating high-volume manufacturing models, but by mastering system integration across multiple material platforms and occupying indispensable positions in the integration value chain.

Why This Matters Now

Between 2026 and 2028, AI-driven system-level integration constraints increasingly shape the evolution of electronic systems, though their impact and timing vary by application domain. Hyperscale data centers and AI infrastructure encounter board- and interconnect-level limits earliest, driving rapid adoption of advanced chip packaging and photonic integration. Edge, industrial, and IoT systems follow different trajectories, shaped more by cost, power, and form-factor constraints, but ultimately face similar integration challenges as scale and functionality increase. Across these domains, the common trend is a gradual relocation of bottlenecks, and therefore strategic leverage, from boards and individual components toward advanced chip packaging, photonics integration, testing, and Beyond-PCB technologies, which increasingly consolidate into long-term industrial control points.

As these integration layers consolidate into strategic control points, actors without system-level integration capabilities risk structural dependence as system control concentrates. Manufacturing cost alone is already not a viable competitive strategy for Europe. Competitive advantage instead arises from technology-intensive manufacturing tightly coupled to design and demanding end-users, supported by sustained R&D and clear strategic focus. Executed coherently, this enables Europe and the Netherlands to shape future optoelectronic system architectures rather than depend on them.

5. Policy Roadmap: From Invention to Industrial Uptake

In this rapidly developing arena, the window to capture strategic control points is closing fast. Around the world, governments and industries are accelerating investments in advanced chip packaging, system integration, and enabling infrastructure, recognizing these as strategic foundations for AI-driven economies. For Europe and the Netherlands, delay risks ceding not only market share, but long-term industrial influence. The challenge is accelerating the transition from invention to industrial uptake. By mastering system-level integration of electronic and photonic technologies, Europe can achieve strategic relevance and indispensability within future value chains. This transition requires a fundamental shift in industrial policy: from a primarily chip-centric focus to a system-centric strategy centered on integration, manufacturing execution, and ecosystem coordination. This shift calls for explicit policy choices to address structural bottlenecks that are specific to system-level integration technologies:

- Fragmented value chains: No single actor controls design–integration–manufacturing, making coordination failures likely.
- Scale gap between R&D and industry: Strong pilot capabilities exist, but industrial-scale manufacturing is missing or delayed.
- High co-dependency risk: System integration requires synchronized availability of multiple technologies and suppliers.
- Insufficient lead markets in Europe: Demand for first-of-a-kind integrated systems is not structurally anchored.
- Capital intensity without clear risk-sharing models: Especially acute in advanced chip packaging and heterogeneous integration.

These bottlenecks are not generic to all deep-tech sectors, but are particularly acute in system-level integration, where multi-actor coordination and synchronized scaling are structural requirements.

The following measures can help translate Europe's technological strengths in system integration into durable industrial positions:

A. **Focus (addresses fragmentation):** Europe and the Netherlands need to make deliberate decisions to focus on future electronics system-level integration capabilities tightly coupled to design and demanding end-users, supported by sustained R&D. Define key roadmaps for concrete end-products, for example, European-designed and integrated high-performance compute systems for AI and data-intensive applications, bringing together key European players and technologies. The Dutch National Technology Strategy addresses the key future electronics technologies. The ministry of EZK could further strengthen its impact by focusing on the NTS and aligning innovation instruments accordingly.

B. **Demand (addresses lack of lead markets):** Early commitment from demanding customers in defense, mobility, or AI infrastructure should be actively mobilized, as it is critical for industrial viability - anchoring scale, reliability requirements, and long-term roadmap alignment. This includes leveraging dual-use application domains, where defense, security, and civilian markets jointly create early scale and performance requirements. The concept of Dutch Defence as a launching customer for Future Electronics applications offers clear potential. Initiatives such as the 10x10 program by the MoD and TNO could play an important role in accelerating the pathway to market.

C. **Scale-up (addresses scale gap):** Pilot lines should be positioned as precursors to industrial facilities, accompanied by early commitments to scaling and supply-chain formation. The Netherlands could further strengthen its position by investing in pilot lines as catalysts for Future Electronics high-tech megaclusters, for instance through the development of unique facilities for beyond-PCB and advanced chip technologies. The realization of the Advanced Chip Packaging line (pillar 4 of ChipNL) would be an important step to help valorize the Dutch knowledge base in these areas.

D. **Access models (addresses risk-sharing & coordination failure):** Investments in High-Tech Megaclusters around open foundries, defined as shared, open-access manufacturing and integration facilities that offer standardized processes to multiple external designers and system builders, should be encouraged. Such models can lower entry barriers, enable multi-actor participation, and attract global design players without requiring vertical integration. The Netherlands could explore new arrangements to encourage ecosystem formation around open facilities. For instance, the ministry of EZK could consider developing funding models for research infrastructure that lower barriers for companies to access these facilities, while R&D subsidy instruments could support more flexible consortium formation. This may help Future Electronics ecosystems to evolve into new industries.

Ecosystems in electronics in The Netherlands

Glossary

3D stacking – Vertically stacking chips to improve performance and reduce footprint.

Advanced chip packaging – Technologies that integrate multiple chips and components into a single high-performance package.

Chiplet – A small specialized chip designed to be combined with other chiplets in a package.

Co-Packaged Optics (CPO) – Integration of optical and electronic components within a tightly coupled package to enable high-speed, high-bandwidth, energy-efficient data communication.

Edge Computing – Processing data close to where it is generated rather than in a central data centre.

Foundry – A company that manufactures semiconductor chips designed by others.

Heterogeneous Integration – Combining chips, components, or technologies made with different processes into a single system.

Inference – The use of a trained AI model to generate predictions or decisions from new data.

Integrated Photonics – Technology that uses light instead of electricity to process, transmit, or sense information on a chip.

Interposer (2.5D Interposer) – An intermediate substrate that connects multiple chips within a package.

Lidar – A sensing technology that uses laser light to measure distance and create 3D maps.

Metrology – The science and technology of measurement used to verify manufacturing quality.

Monolithic Chip – A chip in which all functions are integrated onto a single piece of silicon.

Neuromorphic Computing – Computing architectures inspired by how the human brain processes information.

Optical Interconnect – Data communication using light rather than electrical signals.

OSAT – An (Outsourced Semiconductor Assembly and Test) company that packages, assembles, and tests semiconductor devices on behalf of chip manufacturers.

System-in-Package (SiP) – A package that integrates multiple chips and components, often with different functions, into a single system-level solution.